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| Day | Chapter | Topic | No. of lecture | Remark |
| Day-1 | Basic Structure of Computers | Introduction, Computer Types | 1 |  |
| Day-2 | CA and CO and their relationship | 1 |  |
| Day-3 | Von-Neumann Vs Harvard concept | 1 |  |
| Day-4 | Functional units, Basic operational concepts Bus Structures and Types | 1 |  |
| Day-5 | Machine Instructions and Programs | Memory location and Addressing mechanism | 1 |  |
| Day-6 | Big- and Little-Endian schemes | 1 |  |
| Day-7 | Memory operations, Instruction and instruction sequencing | 1 |  |
| Day-8 | Instruction Format, Instruction length (0,1,2,3 address) with problem | 1 |  |
| Day-9 | Different CPU organization | 1 |  |
| Day-10 | Addressing modes 1 | 1 |  |
| Day-11 | Addressing modes 2 | 1 |  |
| Day-12 | Assembly Language | 1 |  |
| Day-13 | Basic Input and Output Operations, Subroutines | 1 |  |
| Day-14 | Additional Instructions (Logic and Shift/Rotate Instructions) | 1 |  |
| Day-15 | Basic Processing Unit | Fundamental concept, Steps taken by CPU | 1 |  |
| Day-16 | Single bus CPU organization, Execution of a complete instruction | 1 |  |
| Day-17 | Control signals required for an instruction | 1 |  |
| Day-18 | Multiple bus CPU organization | 1 |  |
| Day-19 | Design of control unit: Hardwired | 1 |  |
| Day-20 | Design of control unit: Micro programmed | 1 |  |
| Day-21 | TUTORIAL/ACTIVITY | 1 |  |
| Day-22 | Memory Organization | Basic concepts, Memory hierarchy and it’s need | 1 |  |
| Day-23 | Parameters used to measure the performance. | 1 |  |
| Day-24 | Types of memory components., Semiconductor RAM memories | 1 |  |
| Day-25 | Memory Module Design, | 1 |  |
| Day-26 | ROM | 1 |  |
| Day-27 | Cache memories | 1 |  |
| Day-28 | Mapping functions | 1 |  |
| Day-29 | Replacement algorithms | 1 |  |
| Day-30 | Memory Interleaving | 1 |  |
| Day-31 | Memory performance consideration | 1 |  |
| Day-32 | Virtual memory organization. | 1 |  |
| Day-33 | TUTORIAL/ ACTIVITY | 1 |  |
| Day-34 | ALU | Design of Adder (n-bit ripple carry adder, carry look ahead adder) | 1 |  |
| Day-35 | Multiplication of Positive Numbers | 1 |  |
| Day-36 | Signed Operand Multiplication | 1 |  |
| Day-37 | Fast Multiplication | 1 |  |
| Day-38 | Integer Division (Restoring and non-restoring) | 1 |  |
| Day-39 | IEEE Floating-point Numbers and its Operations (Single and double precision) | 1 |  |
| Day-40 | TUTORIAL/ ACTIVITY | 1 |  |
| Day-41 | TUTORIAL/ ACTIVITY | 1 |  |
| Day-42 | I/O Organization | Basics of I/O operations | 1 |  |
| Day-43 | Accessing I/O Devices | 1 |  |
| Day-44 | Memory mapped I/O and I/O mapped I/O | 1 |  |
| Day-45 | Interrupts | 1 |  |
| Day-46 | DMA | 1 |  |
| Day-47 | Interface Circuits | 1 |  |
| Day-48 | Standard I/O Interfaces -PCI Bus, SCSI Bus, USB | 1 |  |
| Day-49 | Flynn’s Classification (SISD,SIMD,MISD,MIMD) | 1 |  |
| Day-50 | RISC vs CISC | 1 |  |

**Syllabus**

**CS 2006 COMPUTER ORGANIZATION AND ARCHITECTURE Cr- 4**

**Basic Structure of Computers**: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Machine Instructions and Programs: Memory Location and Addressing mechanism, Memory Operations, Encoding of machine instructions, Address modes, Instructions, Instruction formats, Instruction length, Assembly Language, Subroutines, Additional Instructions, RISC vs CISC.

**Basic Processing Unit**: Some Fundamental Concepts, Execution of a Complete Instruction, Single and Multiple Bus Organization, Hardwired Control, Micro programmed Control unit.

**Arithmetic**: Design of fast adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division, Floating-point Numbers and Operations.

**Memory System**: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, memory module design, Cache Memories – Mapping Functions, Replacement Algorithms, Memory interleaving, Memory Performance Considerations Virtual Memories.

**Input/ Output Organization**: Basic Input and Output Operations, Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access. Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB, Flynn’s Classification, RISC vs CISC

**Case Study**: IA-32 Register structure, IA-32 addressing modes, IA-32 Instructions, Instruction format, IA-32 Assembly language, Program flow, Logic and shift/Rotate Instructions for IA-32, Programming examples.

**Text Book**

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, TMH, 5th Edition, 2002.

2. M. Morris Mano, Computer System Architecture, Pearson Education India, 3rd Edition

**Reference Book**

1. Computer Organization & Architecture, William Stallings, 7th Edition, PHI, 2006.

2. John P. Hayes, Computer Organization & Architecture, TMH

**Evaluation Methodology:**

Activities: 30 Marks

Mid Semester Exam: 20 Marks

End Semester Exam: 50 Marks

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**Total** 100 Marks